REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 69-90 are pending; Claims 69 and 80 are currently amended; Claims 1-68 are canceled.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 69-79

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As currently amended, independent claim 69 is recited below:

69. A semiconductor chip or wafer comprising:
a semiconductor substrate;
multiple transistors in or on said semiconductor substrate;
an interconnecting metallization structure over said semiconductor substrate;
a passivation layer over said interconnecting metallization structure, wherein an opening in said passivation layer exposes a contact point of said interconnecting metallization structure;
a first metal layer over said contact point, wherein said first metal layer comprises aluminum; and
a second metal layer over said first metal layer, wherein said second metal layer is used to be wirebonded thereto.

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Reconsideration of Claims 69-74 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (US6,544,880) in view of Yanagida (US6,545,355), of Claim 75 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Galloway (US5,783,868), of Claims 76-78 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Weng (US6,720,243), and of Claim 79 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Chikawa et al. (US5,310,699) is respectfully requested.

Applicants respectfully assert that the structure claimed in claim 69 patentably distinguishes over the citation by Akram (US6,544,880) in view of Yanagida (US6,545,355).

Akram (US6,544,880) teaches a semiconductor device 10 comprising a passivation layer 13 over a substrate 11, wherein an opening in the passivation layer 13 exposes a contact point 12'. The semiconductor device 10 further comprises a first metal layer 12''' and a second metal layer 12'' over said first metal layer 12''', wherein said second metal layer 12'' is used to be wirebonded thereto (Fig. 2E).

However, Akram fails to teach said first metal layer 12''' may comprise aluminum.

Yanagida discloses a first metal layer 20a comprising aluminum. *~ Fig. 1 and col. 6, lines 12-13 ~*

The Examiner considers that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Akram to include aluminum as disclosed in Yanagida because it aids in providing high durability. (Col. 3, lines 5-7) Additionally, since Akram and Yanagida are both from the same field of endeavor, the purpose disclosed by Yanagida would have been recognized in the pertinent art of Akram." ~ *See the last two paragraphs on page 3, in the last Office Action mailed Aug. 15, 2006* ~

Applicants respectfully traverse the Examiner's opinion that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Akram to include aluminum as disclosed in Yanagida because it aids in providing high durability", because Yanagida's device fails to improve the durability of wirebonding.

Yanagida teaches "this makes it possible to improve the reliability and durability of a device product on which the semiconductor chip is mounted by the flip-chip mounting method. In summary, according to the semiconductor device of the first aspect of the present invention, it is possible to improve the electric contact characteristic, reliability, and durability of a device product on which the next-generation high speed LSI chip adopting Cu interconnections is mounted by the flip-chip mounting method." ~ *See col. 3, lines 53-61* ~

Yanagida's device improves the durability of a device product on which the next-generation high speed LSI chip adopting Cu interconnections is mounted by the flip-chip mounting method, but fails to improve the durability of wirebonding. It is believed that the

metal layer 20a used for a flip-chip mounting method, in Yanagida's device, is non-analogous to the metal layer 12''' used for a wirebonding method, in Akram's device. Even under the teachings by Akram in view of Yanagida, the semiconductor chip or wafer claimed in Claim 69 can not be attained. Withdrawal of the rejection to Claim 69 under 35 U.S.C. 103(a) is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 69 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 70-79 patently define over the prior art as well.

Response to Claims 80-90

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As currently amended, independent claim 80 is recited below:

80. A semiconductor chip or wafer comprising:
a semiconductor substrate;
multiple transistors in or on said semiconductor substrate;
an interconnecting metallization structure over said semiconductor substrate;
a passivation layer over said interconnecting metallization structure, wherein an opening in said passivation layer exposes a contact point of said interconnecting metallization structure;
a first metal layer over said contact point, wherein said first metal layer comprises aluminum;
a second metal layer over said first metal layer; and
a wire wirebonded over said second metal layer.

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Reconsideration of Claims 80-85 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (US6,544,880) in view of Yanagida (US6,545,355), of Claim 86 rejected under 35

U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Galloway (US5,783,868), of Claims 87-89 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Weng (US6,720,243), and of Claim 90 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Chikawa et al. (US5,310,699) is respectfully requested.

Applicants respectfully assert that the structure claimed in claim 80 patentably distinguishes over the citation by Akram (US6,544,880) in view of Yanagida (US6,545,355).

Akram (US6,544,880) teaches a semiconductor device 10 comprising a passivation layer 13 over a substrate 11, wherein an opening in the passivation layer 13 exposes a contact point 12'. The semiconductor device 10 further comprises a first metal layer 12''' and a second metal layer 12'' over said first metal layer 12''', wherein said second metal layer 12'' is used to be wirebonded thereto (Fig. 2E).

However, Akram fails to teach said first metal layer 12''' may comprise aluminum.

Yanagida discloses a first metal layer 20a comprising aluminum. *~ Fig. 1 and col. 6, lines 12-13 ~*

The Examiner considers that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Akram to include aluminum as disclosed in Yanagida because it aids in providing high durability. (Col. 3, lines 5-

7) Additionally, since Akram and Yanagida are both from the same field of endeavor, the purpose disclosed by Yanagida would have been recognized in the pertinent art of Akram." ~ *See the last two paragraphs on page 3, in the last Office Action mailed Aug. 15, 2006* ~

Applicants respectfully traverse the Examiner's opinion that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Akram to include aluminum as disclosed in Yanagida because it aids in providing high durability", because Yanagida's device fails to improve the durability of wirebonding.

Yanagida teaches "this makes it possible to improve the reliability and durability of a device product on which the semiconductor chip is mounted by the flip-chip mounting method. In summary, according to the semiconductor device of the first aspect of the present invention, it is possible to improve the electric contact characteristic, reliability, and durability of a device product on which the next-generation high speed LSI chip adopting Cu interconnections is mounted by the flip-chip mounting method." ~ *See col. 3, lines 53-61* ~

Yanagida's device improves the durability of a device product on which the next-generation high speed LSI chip adopting Cu interconnections is mounted by the flip-chip mounting method, but fails to improve the durability of wirebonding. It is believed that the metal layer 20a used for a flip-chip mounting method, in Yanagida's device, is non-analogous to the metal layer 12''' used for a wirebonding method, in Akram's device. Even under the teachings by Akram in view of Yanagida, the semiconductor chip or wafer claimed in Claim 80

can not be attained. Withdrawal of the rejection to Claim 80 under 35 U.S.C. 103(a) is respectfully requested.

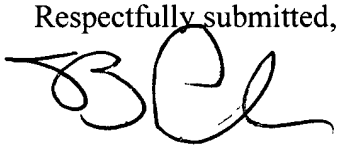
For at least the foregoing reasons, applicants respectfully submit independent claim 80 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 81-90 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Lewis not find that the Claims are now Allowable that she call the undersigned at 845 452-3204 to overcome any problems preventing allowance.

Respectfully submitted,



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